

WHAT IS CLAIMED IS:

1. A method of designing a semiconductor circuit device, comprising the steps of:

generating first circuit data comprising information on a first circuit driven by a voltage from a first power
5 system;

generating second circuit data comprising information on a second circuit driven by a voltage from a second power system different from the first power system;

obtaining cell data prestored in a storage medium and
10 comprising information on a boundary circuit; and

generating boundary circuit connection information indicating that the boundary circuit is connected on a transmission path between the first circuit and the second circuit.

2. A method of designing a semiconductor circuit device according to Claim 1, wherein the boundary circuit comprises a circuit for suppressing short-through current between the first circuit and the second circuit when one
5 of the first circuit and the second circuit is off and another one of the first circuit and the second circuit is on.

3. A method of designing a semiconductor circuit

device according to Claim 1, wherein the boundary circuit comprises a circuit for preventing circuit malfunction due to indeterminate current between the first circuit and the
5 second circuit when one of the first circuit and the second circuit is off and another one of the first circuit and the second circuit is on.

4. A method of designing a semiconductor circuit device according to Claim 1, wherein the boundary circuit comprises a circuit for suppressing leakage current between the first circuit and the second circuit when one of the
5 first circuit and the second circuit is off, and another one of the first circuit and the second circuit is on.

5. A method of designing a semiconductor circuit device according to Claim 1, wherein the boundary circuit comprises a circuit for level conversion between the first circuit and the second circuit.

6. A method of designing a semiconductor circuit device according to Claim 1, wherein the boundary circuit comprises a protection circuit for protecting a transistor in the first circuit and/or the second circuit from
5 electrostatic discharge.

7. A method of designing a semiconductor circuit device according to Claim 1, wherein the first circuit data, the second circuit data, and the cell data are data for logic circuit design.

8. A method of designing a semiconductor circuit device according to Claim 1, wherein the first circuit data, the second circuit data, and the cell data are data for layout design.

9. A semiconductor circuit device designed by a method of designing a semiconductor circuit device according to Claim 1.

10. A method of designing a semiconductor circuit device, comprising the steps of:

designing a first circuit driven by a voltage from a first power system;

5 designing a second circuit driven by a voltage from a second power system different from the first power system; and

connecting a prepared cell on a line for transmitting signals between the first circuit and the second circuit.

11. A semiconductor circuit device designed by a

method of designing a semiconductor circuit device according to Claim 10.

12. A computer-readable storage medium for storing a cell library used for semiconductor design, comprising:

a boundary cell comprising information on a boundary circuit connected on a signal transmission path between a
5 first circuit driven by a voltage from a first power system and a second circuit driven by a voltage from a second power system different from the first power system.

13. A design system for a semiconductor circuit device, comprising:

a unit of generating first circuit data comprising information on a first circuit driven by a voltage from a
5 first power system;

a unit of generating second circuit data comprising information on a second circuit driven by a voltage from a second power system different from the first power system;

a unit of obtaining cell data comprising information
10 on a boundary circuit from the storage medium; and

a unit of generating boundary circuit connection information indicating that the boundary circuit is connected on a transmission path between the first circuit and the second circuit.